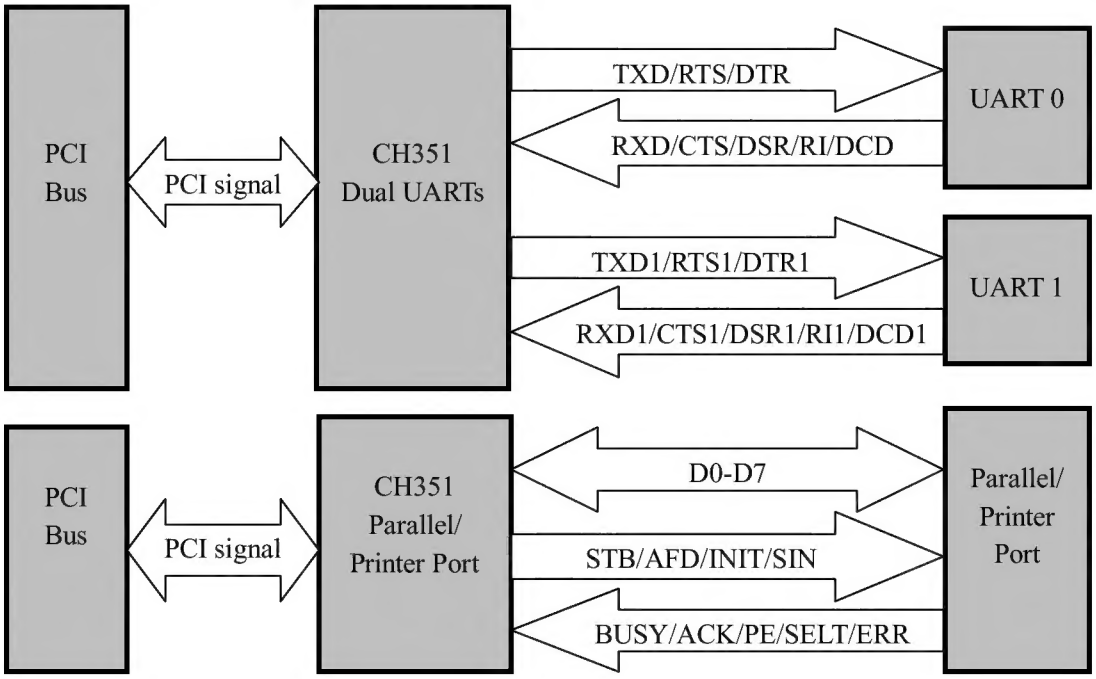
PCI to Dual UARTs or Printer Port Chip CH351

Datasheet (I)
Version: 1A
http://wch.cn

1. Introduction

CH351 is a dual-channel UARTs or printer port chip based on PCI bus, contains dual UARTs which compatible with 16C550, or an EPP/ECP enhanced bi-directional parallel port. The serial port supports half-duplex transmit and receive automatic switching, and supports communication baud rate up to 4Mbps. It can be used for RS232 expansion of PCI bus, PCI high-speed serial port with automatic hardware speed control, serial port networking, RS485 communications, PCI card with parallel/ printer port expansion, etc.

The figure below is general application diagram.



2. Features

2.1. Overview

- The same chip can be configured as dual-channel UARTs, single parallel port/printer port.
- Drive supports Windows 98/ME/NT4.0/2000/XP/Vista/2007/2008 and Linux.
- Supports 5V supply voltage and supports serial port low-power sleep mode.
- Chip function is equivalent to the CH352, providing application solutions such as dual UARTs, quad UARTs, and octal UARTs, etc.
- RoHS compliant LQFP-64 lead-free package.

2.2. Serial Port

- Two fully independent asynchronous serial ports, compatible with 16C450, 16C550 and 16C552 with enhanced.
- Supports 5, 6, 7 or 8 data bits and 1 or 2 stop bits.
- Supports odd, even, none, space 0 and mark 1 parity, etc.
- Programmable communication baud rate, supporting communication baud rate of 115200bps and up to 4Mbps.

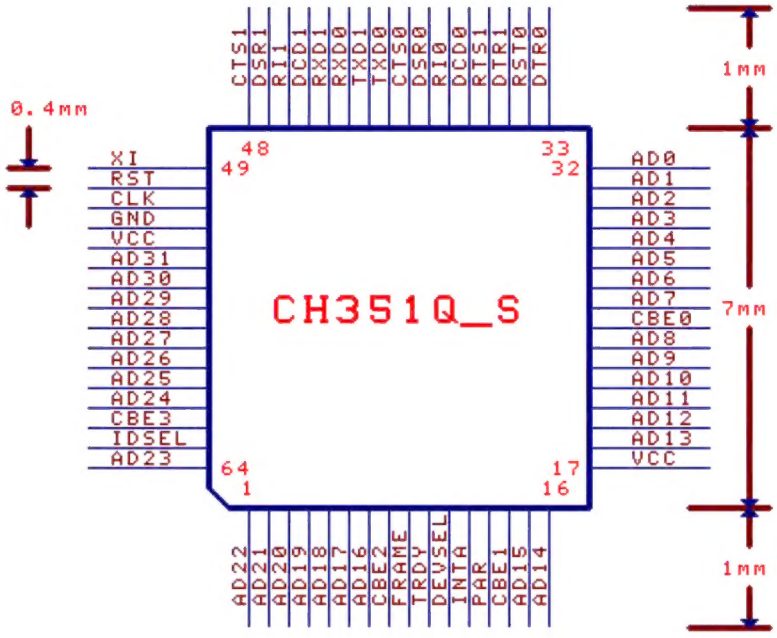
- Built-in 16-byte FIFO buffer, supporting four FIFO trigger layers.
- Supports MODEM signals CTS, DSR, RI, DCD, DTR and RTS, which can be converted to RS232 by 75232.
- Supports automatic handshake and automatic transmission rate control of hardware flow control signals CTS and RTS, compatible with TL16C550C.
- Supports serial frame error check and Break line interval check.
- Supports full-duplex and half-duplex serial communication, providing DTR/TNOW serial port send status signal to support RS485 transmit and receive automatic switching.
- Built-in clock oscillator, optional crystals with frequency such as 22.1184MHz.

2.3. Parallel Port

- Supports SPP, Nibble, Byte, PS/2, EPP, ECP and other IEEE1284 parallel/printer port operation modes.
- Supports bi-directional data transmission and speed can up to 2M Bytes/s.
- Built-in pull-up resistor required for the printer port, fewer peripheral components and simplified circuit.

3. Package

Dual-UART


CH351Q_S
0.4mm
1mm
7mm
1mm
CTS1 DSR1 RI1 DCD1 RXD1 RXD0 TXD1 TXD0 CTS0 DSR0 RI0 DCD0 RTS1 DTR1 RST0 DTR0
XI RST CLK GND VCC AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 CBE3 IDSEL AD23
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 CBE0 AD8 AD9 AD10 AD11 AD12 AD13 VCC
AD22 AD21 AD20 AD19 AD18 AD17 AD16 CBE2 FRAME TRDY DEVSEL INTA PAR CBE1 AD15 AD14
48
49
33
32
64
1
17
16

Refer to the Datasheet (II) CH351DS2.PDF for the application instructions and pins diagram of parallel/ printer port.

Package	Width of Plastic	Pitch of Pin		Instruction of Package	Ordering Information
LQFP-64	7mm x 7mm	0.4mm	15.7mil	small outline LQFP64-pin patch	CH351Q

4. Pin Out

4.1. Power Line and Auxiliary Signal Line

Pin No.	Pin Name	Type	Pin Description
17,53	VCC	Power	Power supply voltage input
52	GND	Power	Ground

49	XI	Input	Input of the crystal oscillator, requires an external crystal

4.2. PCI Bus Signal Line

Pin No.	Pin Name	Type	Pin Description
50	RST	Input/ Output	System reset signal line, active low, and inverted output of crystal oscillation
51	CLK	Input	System clock signal line, active at the rising edge
54-61, 64,1-7, 15-16, 18-23, 25-32	AD31~AD0	Tri-status output and input	Address and bi-directional data multiplexed signal line
62,8, 14,24	CBE3~CBE0	Input	Bus command and byte enable multiplexed signal line
13	PAR	Tri-status and bi-direction	Odd-even parity signal line
63	IDSEL	Input	Initialize device select signal line, active high
9	FRAME	Input	Frame cycle start signal line, active low
10	TRDY	Tri-status output	Target device ready signal line, active low
11	DEVSEL	Tri-status output	Target device select signal line, active low
12	INTA	Open-drain output	INTA interrupt request signal line, active low

4.3. UART0 Signal Line

Pin No.	Pin Name	Type	Pin Description
40	CTS0	Input	MODEM signal, clear to send, active low, built-in weak pull-up
39	DSR0	Input	MODEM signal, data send ready, active low, built-in weak pull-up
38	RI0	Input	MODEM signal, ring indicator, active at low, built-in weak pull-up
37	DCD0	Input	MODEM signal, data carrier detect, active low, built-in weak pull-up
43	RXD0	Input	Received data, built-in weak pull-up
33	DTR0 TNOW0	Output	MODEM signal, data terminal ready, active low TNOW0 is serial data sending status indication, active high
34	RTS0	Output	MODEM signal, request to send, active low
41	TXD0	Output	Transmitted data

4.4. UART1 Signal Line

Pin No.	Pin Name	Type	Pin Description
48	CTS1	Input	MODEM signal, clear to send, active low, built-in weak pull-up
47	DSR1	Input	MODEM signal, data send ready, active low, built-in weak pull-up
46	RI1	Input	MODEM signal, ring indicator, active at low, built-in weak pull-up
45	DCD1	Input	MODEM signal, data carrier detect, active low, built-in weak pull-up
44	RXD1	Input	Received data, built-in weak pull-up
35	DTR1 TNOW1	Output	MODEM signal, data terminal ready, active low TNOW1 is serial data sending status indication, active high
36	RTS1	Output	MODEM signal, request to send, active low
42	TXD1	Output	Transmitted data

5. Configuration

5.1. Global Function Configuration

CH351 is configured with two function modes by RST pin: dual UARTs function mode and parallel/printer port function mode. Refer to the below table.

RST and XI Combination	Function Mode
RST is directly connected to the PCI bus reset signal	Parallel/printer port function mode
RST is connected to the PCI bus reset signal through a resistor A crystal is bridged between XI and RST	Dual UARTs function mode Use external crystal as clock source
RST is connected to the PCI bus reset signal through a resistor XI is directly connected to the PCI bus reset signal	Dual UARTs function mode Use PCI bus clock as clock source

5.2. Internal Clock of Serial Port

There is a clock oscillator inside CH351. Only a crystal is connected between the XI and RST pins to generate the external clock signal required by the serial port. If the crystal is not connected, CH351 can use the PCI bus clock as the external clock signal.

In CH351, the external clock signal of the XI pin performs frequency division or frequency doubling to generate the internal standard clock of UART0 and UART1 respectively. To be compatible with the 16C550 of the existing computer serial port, the default internal clock frequency is 1.8432MHz, and the corresponding maximum baud rate of serial port is 115200bps. CH351 supports multiple internal clock frequencies. When the internal clock frequency is doubled, if the application is unchanged, the actual communication baud rate will be also doubled, namely, the serial port is set to 115200bps by the application, actually, it is 230400bps.

6. Register

6.1. Basic Specification

6.1.1. Abbreviation of Attribute: R=read-only, W=read and write, S=read-only but can be set in advance,…=ellipsis.

6.1.2. Numerical system of data: If it ends with H which is a hexadecimal number. Otherwise, it is a binary number.

6.1.3. Wildcard character and attribute of numeric value: r=reserved (disabled), x=any value,…=ellipsis.

6.2. PCI Configuration Space

Type	Address	Register Name	Register Attribute	Default Value After System Reset
Standard PCI device configuration space	01H-00H	Vendor ID	SSSS	1C00H
	03H-02H	Device ID	SSSS	2273H or 2170H, post-note
	05H-04H	Command	RRRRRRRRRRRRRRRW	0000000000000000
	07H-06H	Status	RRRRRRRRRRRRRRR	000000100000x000
	08H	Revision ID	SS	0FH
	0BH-09H	Class Code	SSSSSS	070002H or 070101H
	0FH-0CH		RRRRRRRR	00000000H
	13H-10H	I/O Base Address 0 (UART0)	WWWWWWWWWWWWWWWW WWWWWWWWWWWWWRRR	0000000000000000 0000000000000001

	17H-14H	I/O Base Address 1 (UART1 or parallel port)	WWWWWWWWWWWWWWWW WWWWWWWWWWWWRRR	0000000000000000 0000000000000001
	2BH-18H		RRRR….RRRR	0000….0000H
	2FH-2CH	Subsystem ID	SSSSSSSS	Same as DID+VID
	3BH-30H		RRRR….RRRR	0000….0000H
	3FH-3CH	Interrupt Line & Pin	RRRRRRRRRRRRRRRR RRRRRRRRWWWWWWWW	0000000000000000 0000000100000000
Configuration register	40H	Configuration control register CFG_CTRL	RRRRRRWW	0x100011
	7FH-41H	Reserved	(Disabled)	(Disabled)

DID device identification of the configuration space is 2273H in dual UARTs function mode and 2170H in parallel/printer port function mode; CC device class code is 070002H in dual UARTs function mode and 070101H in parallel/printer port function mode.

6.3. Bit of Configuration Register

Register Name	Address	Attribute	Instruction For Use Of Bit	Value=0	Value=1
Configuration control register CFG_CTRL (Configuration space 40H address)	Bit 0	W	Bit variable register		
	Bit 1	W	Bit variable register		
	Bit 6	R	Current global function mode status	Dual UART	Parallel port

6.4. Serial Port Register

The serial Port of CH351 is compatible with the industry standard 16550 with enhanced. The register bit marked in gray in the table is the enhanced function, and other registers refer to the description of the single serial port 16C550 or dual UARTs CH432. The actual address of the UART 0 register is the I/O base address 0 adds the offset address in the table, and the actual address of the UART 1 register is the I/O base address 0 adds the offset address in the table. Excluding SLP/CK2X register, the registers of UART0 and UART1 are the same. In the table, DLAB is bit 7 of the LCR register , X indicates that the value of DLAB is not concerned, RO indicates that the register is read-only, WO indicates that the register is write-only, and R/W indicates that the register is readable and writable.

Address	DLAB	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	RO	RBR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	WO	THR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	R/W	IER	RESET	LOWPOWER	SLP/CK2X	0	IEMODEM	IELINES	IETHRE	IERECV
2	X	RO	IIR	FIFOENS	FIFOENS	0	0	IID3	IID2	IID1	NOINT
2	X	WO	FCR	RECVTG1	RECVTG0	0	0	0	TFIFORST	RFIFORST	FIFOEN
3	X	R/W	LCR	DLAB	BREAKEN	PARMODE1	PARMODE0	PAREN	STOPBIT	WORDSZ1	WORDSZ0
4	X	R/W	MCR	HALF	TNOW	AFE	LOOP	OUT2	OUT1	RTS	DTR
5	X	RO	LSR	RFIFOERR	TEMT	THRE	BREAKINT	FRAMEERR	PARERR	OVERR	DATARDY
6	X	RO	MSR	DCD	RI	DSR	CTS	ΔDCD	ΔRI	ΔDSR	ΔCTS
7	X	R/W	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	R/W	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	R/W	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

The following table shows the default value of the serial port register after the power-on reset or PCI bus reset or serial port soft reset.

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IER	0	0	0	0	0	0	0	0
IIR	0	0	0	0	0	0	0	1
FCR	0	0	0	0	0	0	0	0
LCR	0	0	0	0	0	0	0	0
MCR	0	0	0	0	0	0	0	0
LSR	0	1	1	0	0	0	0	0
MSR	DCD	RI	DSR	CTS	0	0	0	0
SCR	Keep	Keep	Keep	Keep	Keep	Keep	Keep	Keep
FIFO	Reset, including transmitter FIFO and receiver FIFO							
TSR	Reset; TSR is the serial port transmitter shift register							
RSR	Reset; RSR is the serial port receiver shift register							
Other	Undefined							

RBR: receiver buffer register. If the DATARDY bit of LSR is 1, the received data can be read from this register. If FIFOEN is 1, the data received from the serial port shift register RSR is firstly stored in the receiver FIFO, and then read out through this register.

THR: transmitter holding register, including transmitter FIFO, used to write the data to be transmitted. If FIFOEN is 1, the written data is firstly stored in the transmitter FIFO, and then output one by one through the transmitter shift register TSR

IER: interrupt enable register, including enhanced function control bit and serial port interrupt enabling.

RESET: bit=1, soft reset the serial port, and this bit can be cleared to 0 automatically without software clearing.

LOWPOWER: bit=1, the internal standard clock of the serial port is turned off, so that the serial port enters a low-power status.

SLP/CK2X: the use of this bit of UART0 and UART1 is different, and the UART0 is SLP. When the bit is 1, turn off the clock oscillator, so that both the UART0 and UART1 will sleep. The UART1 is CK2X. When the bit is 1, force the external clock signal to frequency doubling and then use it as the internal standard clock of UART0 and UART1.

IEMODEM: bit =1, which allows modem input status change interrupt.

IELINES: bit =1, which allows received line status interrupt.

IETHRE: bit =1, which allows null interrupt for transmitter holding register.

IERECV: bit =1, which allows received data interrupt.

IIR: interrupt identification register, used to analyze and process the interrupt source.

FIFOENS: this bit is the FIFO enabled status, and 1 means that the FIFO has been enabled..

IIR Register Bit				Priority	Interrupt Type	Interrupt Sources	Clear Interrupt Method
IID3	IID2	IID1	NOINT				
0	0	0	1	None	No interrupt	No interrupt	
0	1	1	0	1	Receive line status	OVERR, PARERR, FRAMEERR, BREAKINT	Read LSR
0	1	0	0	2	Received data available	The number of bytes received reaches to the trigger point of FIFO	Read RBR
1	1	0	0	2	Received data timeout	Next data is not received when the time of more than four data	Read RBR
0	0	1	0	3	THR register null	Transmitter holding register null, IETHRE changes from 0 to 1 which can re-enable the interrupt	Read IIR Or write THR

0	0	0	0	4	MODEM input change	ΔCTS, ΔDSR, ΔRI, ΔDCD	Read MSR

FCR: first-in-first-out buffer FIFO control register, used to enable and reset FIFO.

RECVTG1 and RECVTG0: setting the trigger point interrupt of receiver FIFO and the trigger point of hardware flow control. 00 corresponds to 1 byte, namely, available interrupt of received data is generated when 1 byte is received, and RTS pin is automatically invalid when enabling hardware flow control. 01 corresponds to 4 bytes, 10 corresponds to 8 bytes, 11 corresponds to 14 bytes.

TFIFORST: bit=1, clearing the data in the transmitter FIFO (not including TSR), this bit can be cleared to 0 automatically without software clearing.

RFIFORST: bit=1, clearing the data in the transmitter FIFO (not including RSR), this bit can be cleared to 0 automatically without software clearing.

FIFOEN: bit=1, enabling FIFO, this bit is cleared to 0, FIFO will be disabled. After FIFO is disabled, it will be 16C450 compatible mode, which is equal to only one byte in FIFO

LCR: line control register, used to control the format of serial communication.

DLAB: this bit is the divisor latch access enable. When it is 1, DLL and DLM can be accessed; when it is 0, RBR/THR/IER can be accessed.

BREAKEN: bit=1, it is forced to generate a BREAK line interval.

PARMODE1 and PARMODE0: when PAREN is 1, setting the format of the odd-even parity bit: 00 means odd parity, 01 means even parity, 10 means mark bit (MARK, set to 1), 11 means space bit (SPACE, cleared to 0).

PAREN: bit=1, it is allowed to generate parity bit during transmitting and to check parity bit during receiving. If it is 0, there is no parity bit.

STOPBIT: bit=1, two stop bits; bit= 0, one stop bit.

WORDSZ1 and WORDSZ0: setting the byte length; 00 means 5 data bits, 01 means 6 data bits, 10 means 7 data bits, and 11 means 8 data bits.

MCR: MODEM control register, used to control MODEM output

HALF: bit=0, it will work in full-duplex communication mode, and the transmitting and receiving can be done independently at the same time; bit=1, it will work in half-duplex communication mode, and the receiving will be automatically turned off during transmitting until the transmission is completed.

TNOW: bit=1, the DTR pin will be renamed to TNOW pin, which is used to indicate the status of serial data being transmitted, active high. It can be used to automatically control the RS485 transceiver switch in half-duplex serial application.

AFE: bit=1, the hardware automatic flow control of CTS and RTS is allowed. If AFE is 1, then the serial port will continue to send the next data only when it detects that the CTS pin input is valid (active low), otherwise, suspended. The CTS input status change will not generate the MODEM status interrupt when AFE is 1. If AFE is 1 and RTS is 1, the serial port will automatically validate the RTS pin (active low) when receiver FIFO is null, and the serial port will automatically invalidate the RTS pin until the number of received bytes reach the trigger point of FIFO , and will re-validate the RTS pin when the receiver FIFO is null. Through the hardware automatic band rate control, the CTS pin connects to the other's RTS pin, the RTS pin connects to the other's CTS pin.

LOOP: bit=1, enabling test mode of the internal loop. In the test mode, all external output pins of the serial port are at the invalid status, TXD internally returns to RXD (namely, TSR output internally returns to RER input), RTS internally returns to CTS, DTR internally returns to DSR, OUT1 internally returns to RI and OUT2 internally returns to DCD.

OUT2: bit=1, the interrupt request output of the serial port is allowed, otherwise, the serial port will not generate the actual interrupt request.

OUT1: bit is a user-definable MODEM control bit, and the actual output pin is not connected.
RTS: bit=1, the RTS pin output is valid (active low), otherwise, the RTS pin output is invalid.
DTR: bit=1, the DTR pin output is valid (active low), otherwise, the DTR pin output is invalid.

LSR: line status register, used to query and analyze the status of the serial port.
RFIFOERR: bit=1, it means that there is at least one PARERR, FRAMEERR or BREAKINT error in the receiver FIFO.
TEMT: bit=1, it means that the transmitter holding register (THR) and the transmitter shift register (TSR) are empty.
THRE: bit=1, it means that the transmitter holding register (THR) is empty.
BREAKINT: bit=1, it means that the BREAK line interval is detected.
FRAMEERR: bit=1, it means the frame error of the data which being read from the receiver FIFO, and it lacks a valid stop bit.
PARERR: bit=1, it means the odd-even parity error of the data which being read from the receiver FIFO.
OVERR: bit=1, it means that the receiver FIFO buffer has overflowed.
DATARDY: bit=1, it means that there is received data in the receiver FIFO. After reading all the data in the FIFO, this bit will be automatically cleared to 0.

MSR: MODEM status register, used to query the Modem status.
DCD: this bit is bit reverse of the DCD pin, bit=1, it means that the DCD pin is valid (active low).
RI: this bit is bit reverse of the RI pin, bit=1, it means that the RI pin is valid (active low).
DSR: this bit is bit reverse of the DSR pin, bit=1, it means that the DSR pin is valid (active low).
CTS: this bit is bit reverse of the CTS pin, bit=1, it means that the CTS pin is valid (active low).
ΔDCD: bit=1, it means that the DCD pin input status has changed.
ΔRI: bit=1, it means that the input status of the RI pin has changed.
ΔDSR: bit=1, it means that the input status of the DSR pin has changed.
ΔCTS: bit=1, it means that the input status of the CTS pin has changed.

SCR: user can define register.

DLL and DLM: baud rate divisor latch. DLL is the low byte and DLM is the high byte, The 16-bit divisor formed by both which is used for the serial port baud rate generator composed by a 16-bit counter. The divisor = the internal standard clock of the serial port / 16 / the required communication baud rate. If the internal standard clock of the serial port is 1.8432MHz and the required baud rate is 9600bps, then the divisor =1843200/16/9600=12.

7. Functional Description

7.1. Query and Interrupt

The dual-UARTs of CH351 share a PCI interrupt request pin, so after entering the PCI interrupt service, firstly analyzing whether it is ch351 request interrupt, and which UART. After entering the interrupt service, firstly read the IIR register of UART0. If there is an interrupt, process and exit it; if there is no interrupt, read the IIR register of UART1; if there is an interrupt, process and exit it, and if there is no interrupt, exit it directly. After ensuring that it is an interrupt of a certain UART, you can further analyze the LSR register, analyze the cause of the interrupt and process it if necessary.

If the serial port works in the interrupt mode, then setting the IER register to allow the corresponding interrupt request, and set OUT2 of the MCR register to allow interrupt output.

If the serial port works in query mode, then no need to set OUT2 of IER and MCR, and only need to query the LSR register, and analyze and process it.

7.2. Serial Port Operation

For specific operations, please refer to the specifications of single serial port 16C550 or dual UARTs CH432.

7.3. Application Specification

The serial port's output pins of CH351 are all CMOS level, and compatible with TTL. The input pins can be compatible with CMOS and TTL. It can be further converted to RS232 by adding an RS232 conversion chip externally.

When the serial port of CH351 works normally, the clock signal shall be externally provided for XI pin. Generally, the clock signal is generated by the built-in inverter of CH351 through the crystal stable frequency oscillator. After PCI bus reset, bit 0 of the command register of the PCI configuration space is 0 (I/O space disabling), so CH351 will automatically turn off the clock oscillator, so that both UART 0 and UART 1 will enter the sleep status. Not starting clock oscillator until CH358 is assigned with I/O base address and the bit 0 of the command register is 1.

The pins of CH351 in UART mode include: data transmission pin and MODEM signal pin. The data transmission pins include: TXD and RXD, both are at high level by default. The MODEM signal pins include: CTS, DSR, RI, DCD, DTR and RTS, all are at high level by default. All MODEM signals can be used as general-purpose IO pins, controlled and defined usage by the computer application.

CH351 has built-in independent transceiver buffer and FIFO, supporting simplex, half-duplex or full duplex asynchronous serial communication. Serial data includes one low-level start bit, 8 data bits, 0 or 1 additional parity bit or flag bit; 1 or 2 high-level stop bits, and supports odd/even/mark/space parity. CH351 supports common communication baud rates: 1200, 2400, 4800, 9600, 19.2K, 38.4K, 57.6K, 115.2K, 230.4K, 460.8K, 921.6K, 1.8432M, 2.7648M, etc. The baud rate error of the serial port transmitting signal is less than 0.2%, and the allowable baud rate error of the serial port receiving signal is not less than 2%.

In Windows and Linux OS, the drive of CH351 can be compatible with standard serial ports, so most of the original serial port applications are completely compatible and without any modification.

CH351 can be used to expand additional high-speed RS232 for computer through PCI bus, and support high baud rate serial port with automatic hardware speed control, RS422 or RS485 communication interface, etc.

8. Parameters

8.1. Absolute Maximum Ratings

(Critical state or exceeding maximum can cause chip to not work or even be damaged)

Name	Parameter Description	Min	Max	Unit
TA	Operating ambient temperature	-40	85	℃
TS	Storage ambient temperature	-55	125	℃
VCC	Supply voltage (VCC connects to power, GND to ground)	-0.5	6.0	V
VIO	Voltage of the input or output pins	-0.5	VCC+0.5	V

8.2. Electrical Parameters

(Test Conditions: TA=25℃, VCC=5V, exclude pins connected to PCI bus)

Name	Parameter Description	Min	Typ.	Max	Unit
VCC	Supply voltage (please refer to the attention below)	4.5	5	5.3	V
ICC	Operating supply current	1	15	50	mA
VIL	Input low voltage	-0.5		0.8	V
VIH	Input high voltage	2.0		VCC+0.5	V
VOL	Output low voltage (4mA draw current)			0.5	V
VOH	Output high voltage (1mA output current)	VCC-0.5			V

IIN	Input current of the input without pull-up			10	uA
IUP	Input current of the input with weak pull-up	3	8	200	uA

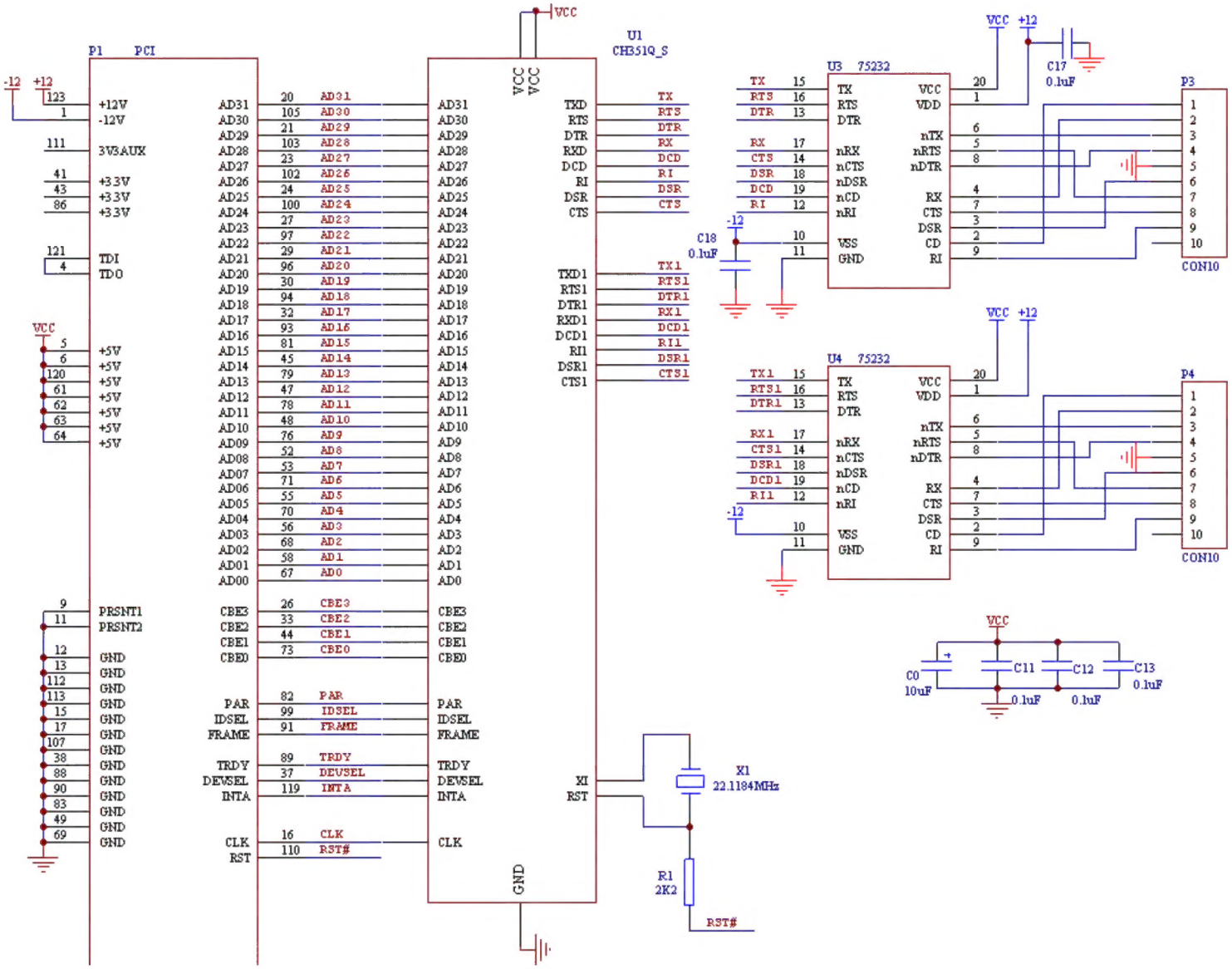
8.3. Timing Parameters

(Test Conditions: TA=25℃, VCC=5V, FCLK=33.3MHz, refer to the figure)

Name	Parameter Description	Min	Typ.	Max	Unit
FCLK	CLK input frequency (main frequency of PCI bus)	0	33.3	40	MHz
FXI	XI input frequency, crystal frequency	0.9216	22.1184	33.3	MHz

9. Applications

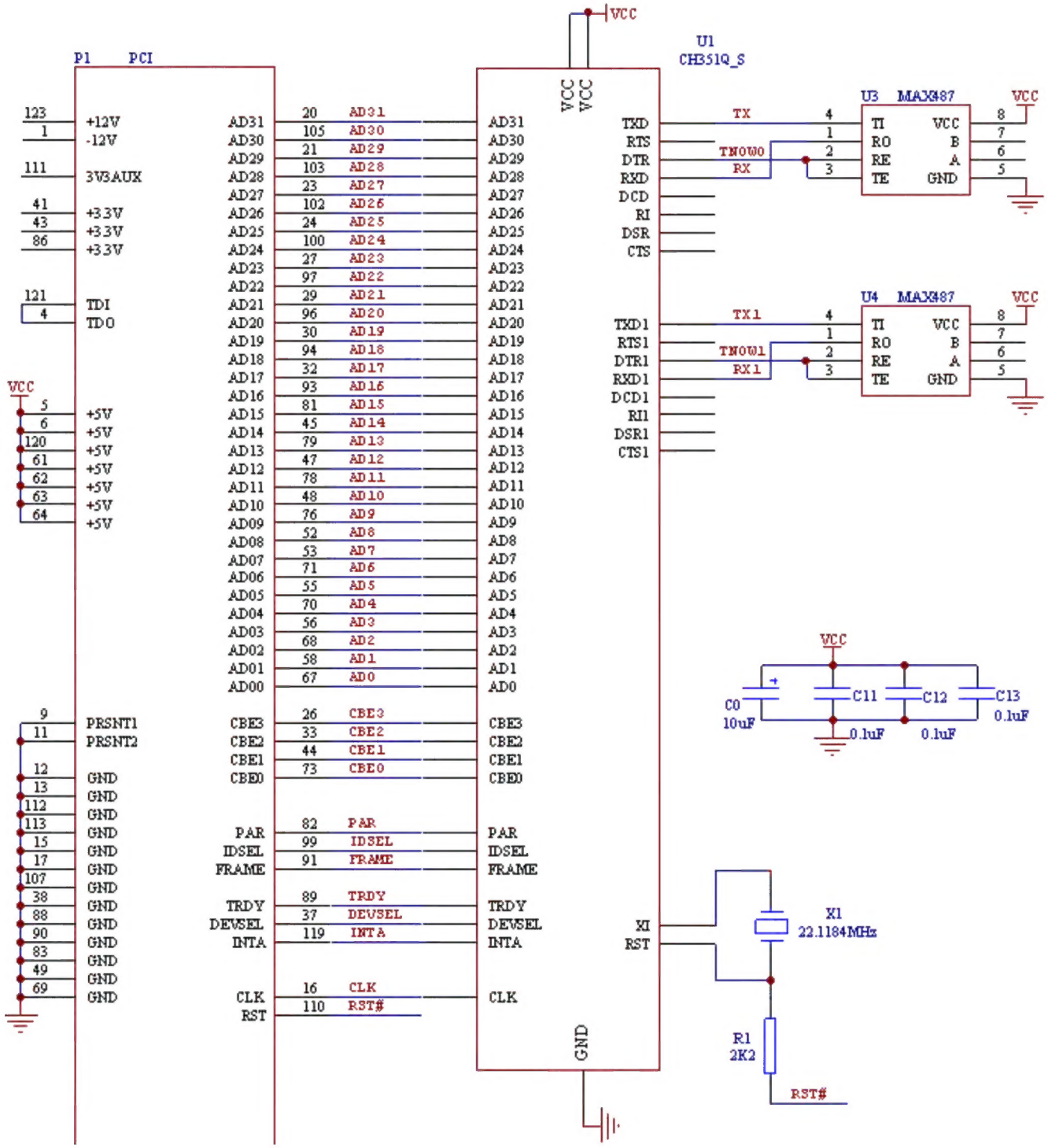
9.1. Dual-RS232 Serial Port



This is a PCI dual-channel serial port circuit based on the CH351. U3 and U4 are RS232 conversion chip 75232, P3 and P4 are 10-pin double-row or DB9 pins. Crystal X1 is used for the clock oscillation circuit. Capacitor C0 and C11～C13 are used for power decoupling, C11～C13 are monolithic or high-frequency ceramic capacitors with a capacity of 0.1uF. They are connected in parallel nearby to the power pins of

CH351 or 75232 separately.

CH351 is a high-frequency digital circuit, so signal impedance matching shall be considered. Please refer to PCI bus specification when designing the PCB board. It is recommended that the length of PCI signal line of CH351 shall be less than 35mm and the length of the clock line CLK try to be between 50mm~65mm, and it shall not be close to other signal lines. It is recommended to arrange ground or copper on both sides of CLK and on the back of the PCB to reduce signal interference from the outside.

9.2. Dual-RS485 Interface

This is a PCI dual-RS485-interface circuit based on CH351, U3 and U4 are RS485 transceiver chips.